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A NOVEL TECHNIQUE FOR GROUND BOUNCE NOISE REDUCTION IN DEEP SUB MICRON CIRCUITS

K ASHOK REDDY
M.Tech (VLSI)
Mannan Institute of Science & Technology

B.SUNIL KUMAR
Associate Professor & HOD
Mannan Institute of Science & Technology

Abstract: **As low power circuits area unit we have a tendency toll liked preferred most well-liked} currently a days because the scaling increase the leak powers within the circuit conjointly will increase chop-chop therefore for removing these quite leakages and to produce a stronger power potency we area unit exploitation many sorts of power gating techniques. during this paper we tend to area unit aiming to analyze totally different the various} varieties of flip-flops using differing types of power gated circuits exploitation low power VLSI style techniques and that we area unit aiming to show the comparison results between different micromillimetre technologies. The simulations were done exploitation Micro wind Layout Editor & DSCH software package and therefore the results got below.**

I. INTRODUCTION

The scaling of method technologies to nanometer regime has resulted during a speedy increase in outflow power dissipation. Hence, it's become very vital to develop style techniques to scale back static power dissipation during times of inactivity. The facility reduction should be achieved while not trading-off performance that makes it tougher to scale back outflow throughout traditional (runtime) operation. On the opposite hand, there are many techniques for reducing outflow power in sleep or standby mode. Power gating is one such standard technique wherever a sleep semiconductor unit is side between actual ground rail gate grounds (called virtual ground). This device is turned-off within the sleep mode to cut-off the outflow path. It's been shown that this method provides a considerable reduction in outflow at a stripped impact on performance.

Power gating technique uses high Green Mountain State sleep transistors that interrupt VDD from a circuit block once the block isn't switch. The sleep semiconductor unit size is a very important style parameter. this method, additionally referred to as MTCMOS, or Multi-Threshold CMOS reduces stand-by or outflow power, and additionally permits did testing.

Power gating affects style design quite clock gating. It will increase time delays as power gated modes need to be safely entered and exited. Subject area trade-offs exist between coming up with forth quantity of outflow power saving in low power modes and also the energy dissipation to enter and exit the low power modes. closing down the blocks are often accomplished either by code or hardware. Driver code will schedule the facility down operations. Hardware timers are often utilized. A fanatical power management controller is another choice.

An outwardly switched power offer may be a terribly basic variety of power gating to realize future outflow power reduction. To shut off the block for little intervals of your time, internal power gating is a lot of appropriate. CMOS switches that give power to the electronic equipment are controlled by power gating controllers. Outputs of the facility gated block discharge slowly. thus output voltage levels pay longer in threshold voltage level. This will cause larger short current.

Power gating uses low-leakage PMOS transistors as header switches to shut off power provides to parts of a style in standby or sleep mode. NMOS footer switches also can be used as sleep transistors. Inserting the sleep transistors splits the chip's power network into a permanent power network connected to the facility offer and a virtual power network that drives the cells and might be turned off.

The quality of this advanced power network is important to the success of a power-gating style. 2 of the foremost important parameters are the IR-drop and also the penalties in atomic number 14 space and routing resources. Power gating are often enforced exploitation cell- or cluster-based (or fine grain) approaches or a distributed coarse-grained approach.

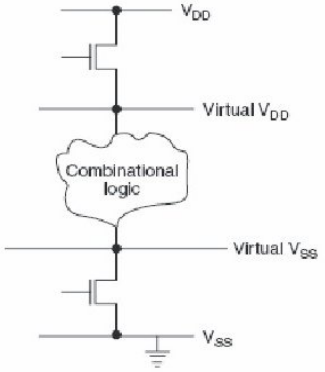

Fig1: Power Gated Circuits

II. POWER-GATING PARAMETERS

Power gating implementation has further issues for temporal order closure implementation. the subsequent parameters got to be thought of and their values rigorously chosen for a undefeated implementation of this technique.

1) Power gate size: the facility gate size should be chosen to handle the quantity of shift current at any given time. The gate should be larger such there's no measurable voltage (IR) drop because of the gate. As a rule of thumb, the gate size is chosen to be around three times the shift capacitance. Designers may choose from header (P-MOS) or footer (N-MOS) gate. Sometimes footer gates tend to be smaller in space for a similar shift current. Dynamic power analysis tools will accurately live the shift current and additionally predict the scale for the facility gate.
2) Gate management slew rate: In power gating, this is often a crucial parameter that determines the facility gating potency. Once the slew rate is massive, it takes longer to modify off and switch-on the circuit and thus will have an effect on the facility gating potency. Slew rate is management led through buffering the gate control signal.
3) Co-occurring shift capacitance: This vital constraint refers to the quantity of circuit that may be switched at the same time while not touching the facility network integrity. If an oversized quantity of the circuit is switched at the same time, the ensuing "rush current" will compromise the facility network integrity. The circuit must be switched piecemeal so as to forestall this.
4) Power gate leakage: Since power gates are made from active transistors, outpouring reduction is a crucial thought to maximize power savings.

i) Fine-grain power gating

Adding a sleep junction transistor to each cell that's to be turned off imposes an oversized space penalty, and on an individual basis gating the facility of each cluster of cells creates temporal order problems introduced by inter-cluster voltage variation that are troublesome to resolve. Fine-grain power gating encapsulates the shift junction transistor as a district of the quality cell logic. Shift transistors are designed by either the library information processing marketer or primary cell designer. Sometimes these cell styles adapt to the traditional primary cell rules and might simply be handled by EDA tools for implementation.

The size of the gate management is intended considering the worst case state of affairs that may need the circuit to modify throughout each clock cycle, leading to a large space impact. a number of the recent styles implement the fine-grain power gating by selection, however just for the low Vermont cells. If the technology permits multiple Vermont libraries, the utilization of low Vermont devices is minimum within the style (20%), in order that the realm impact is reduced. once mistreatment power gates on the low Vermont cells the output should be isolated if succeeding stage may be a high Vermont cell. Otherwise it will cause the neighboring high Vermont cell to possess outpouring once output goes to associate degree unknown state because of power gating.

Gate management slew rate constraint is achieved by having a buffer distribution tree for the management signals. The buffers should be chosen from a group of invariably on buffers (buffers while not the gate management signal) designed with high Vermont cells. The inherent distinction between once a cells switches off with reference to another, minimizes the push current throughout switch-on and switch-off.

Usually the gating junction transistor is intended as a high Vermont device. Coarse-grain power gating offers additional flexibility by optimizing the facility gating cells wherever there's low shift activity. outpouring improvement should be done at the coarse grain level, swapping the low outpouring cell for the high outpouring one. Fine-grain power gating is a chic methodology leading to up to ten times outpouring reduction. this sort of power reduction makes it associate degree appealing technique if the facility reduction demand isn't glad by multiple Vermont improvement alone.

ii) Coarse-grain power gating

The coarse-grained approach implements the grid vogue sleep transistors that drive cells domestically through shared virtual power networks. This approach is a smaller amount sensitive to PVT variation, introduces less IR-drop variation, and imposes a smaller space overhead than the cell- or cluster-based implementations. In coarse-grain power gating, the facility-gating junction transistor may be a part of the power distribution network instead of the quality cell.

There are 2 ways that of implementing a coarse-grain structure:

1) Ring-based: the facility gates are placed round the perimeter of the module that's being switched-off as a hoop. Special corner cells are accustomed flip the facility signals round the corners.

2) Column-based: the facility gates ar inserted within the module with the cells abutted to every different within the variety of columns. The world power is that the higher layers of metal, whereas the switched power is within the lower layers.

Gate filler depends on the general shift current of the module at any given time. Since solely a fraction of circuits switch at any purpose of your time, power gate sizes are smaller as compared to the fine-grain switches. Dynamic power simulation mistreatment worst case vectors will confirm the worst case shift for the module and thus the scale. The IR drop may be factored into the analysis. Co-occurring shift capacitance may be a major thought in coarse-grain power gating implementation. so as to limit co-occurring shift, gate management buffers is flower enchained, and special counters is accustomed by selection activate blocks of switches.

III. POWER GATING FOR DELAY REDUCTION

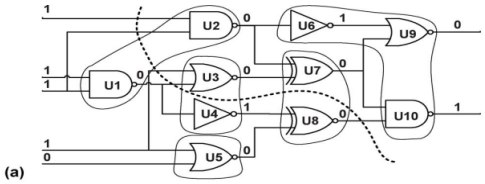

Fig2: Device without Power gating.

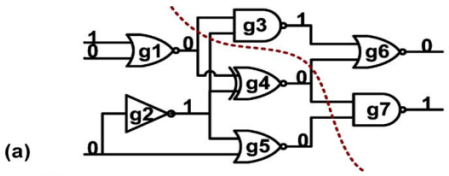

Fig3: Device with Power gating with reduced area & Power using clustering network formation.

This work presented a logic clustering based solution to the problem of controlling/optimizing the power gating parameters. The key design considerations in the power mode transitions are minimizing the wakeup delay, the peak current, and the total size of sleep transistors. This work analyzed the relations between the three parameters, and solved the problem of finding logic clusters and their wakeup schedule that minimize the wakeup delay while satisfying the peak current and performance loss constraints.

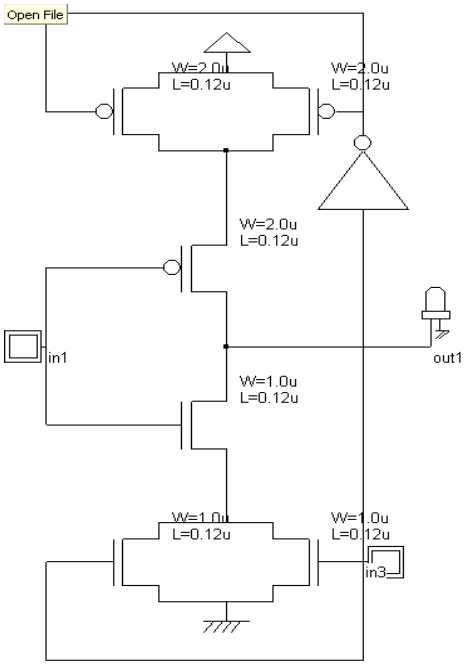

Fig4: Sleepy stack

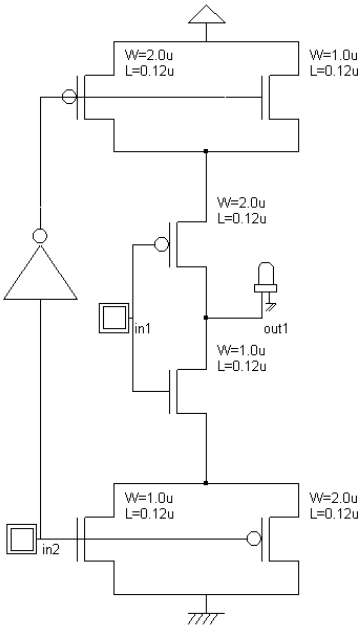

Fig5: Dual Sleep Method

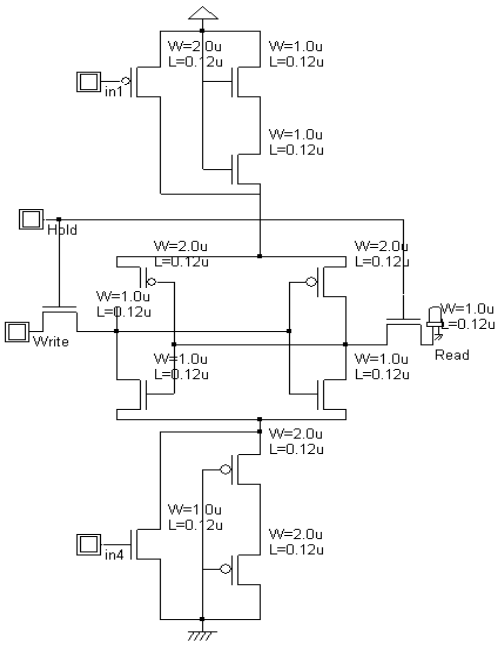

Fig6: Du al Stack Approach

A variation of the sleep approach, the zigzag approach, reduces wake- up overhead caused by sleep transistors by placement of alternating sleep transistors presumptuous a specific pre-selected input vector [6]. Another technique for outpouring power reduction is that the stack approach, that forces a stack impact by breaking down Associate in Nursing existing semiconductor into 2 [*fr1] size transistors [7]. The divided transistors increase delay considerably and will limit the utility of the approach. The sleepy headed stack approach (Fig. 2) combines the sleep and stack approaches [2, 3]. The sleepy headed stack technique divides existing transistors into 2 [*fr1] size transistors just like the stack approach. Then sleep transistors are more in parallel to 1 of the divided transistors. Throughout sleep mode, sleep transistors are turned off and stacked transistors suppress outpouring current whereas saving state. Every sleep semiconductor, placed in parallel to the one among the stacked transistors, reduces resistance of the trail, thus delay is shriveled throughout active mode. However, space penalty could be a vital matter for this approach since each semiconductor is replaced by 3 transistors and since further wires are more for S and S', that are sleep signals. Another technique referred to as twin sleep approach [8] (Fig. 3) uses the advantage of victimization {the 2|the 2} additional pull- up and two additional pull-down transistors in sleep mode either in OFF state or in ON state. Since the twin sleep portion will demanded common to any or all logic electronic equipment, less range of transistors is required to use an exact logic circuit.

The variations between these 3 power gating techniques are checked by coming up with a flip-flop's then simulated victimization the tools and snapshots are given below are given below. As flip-flops are most ordinarily employed in all the digital circuits it's a lot of required to create the flip-flops a lot of power economical than all different devices. during this half we have a tendency to are coming up with the low power flip-flops by reducing the ability victimization power gated technology. The new flip-flop design's victimization twin Stack technique is shown below. the twin stack technique has noise potency & power potency than traditional flip-flops.

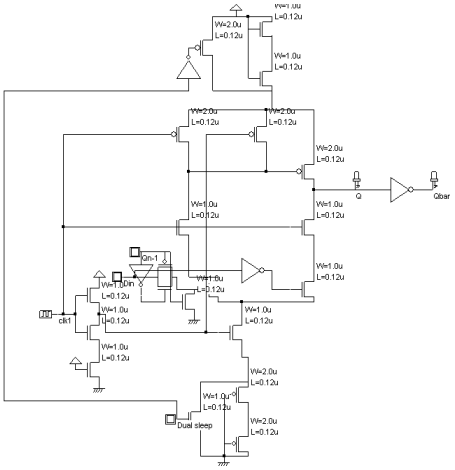

Fig7: Conventional CDMFF Flip-flop using Power Gated Circuits

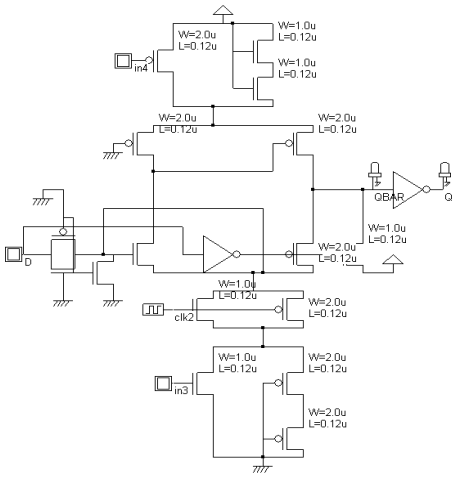

Fig 8: SCCER Flip-Flop using Power Gated Circuits

IV. TABULATION RESULTS

Type	Area	Power
CDMFF	390um	0.271mW
CDMFF with Dual Stack	630um	0.185mW

Thus the Dual stack method shows much reduced power than all the circuits. But the area constraints have been considerably increased. But using scaling techniques we can improve the area constraints.

V. CONCLUSION

In metric linear unit scale CMOS technology, sub threshold escape power consumption could be a nice challenge. Though previous approaches area unit effective in some ways in which, no good resolution for reducing escape power consumption is nonetheless renowned. Therefore, designers opt for techniques primarily based upon technology and style criteria. During this paper, we offer novel circuit structure named "Dual stack" as a brand new remedy for designers in terms of static power and dynamic powers. In contrast to the sleep semiconductor unit technique, the twin stack technique retains the first state. The twin stack approach shows the smallest amount speed power product among all strategies. Therefore, the twin stack technique provides new ways in which to designers that need ultra-low escape power consumption with a lot of less speed power product. Particularly it shows nearly 50-60% of power than the present traditional or standard flip-flops. So, it is used for future integrated circuits for power & space potency.

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